

ATM3201/ATM3221

Extreme Low Power Bluetooth 5.0 SoC with Energy Harvesting



Product Brief

Overview

The ATM3201/ATM3221 is part of a family of extreme low-power Bluetooth® 5 system-on-a-chip (SoC) solutions. This Bluetooth Low Energy SoC integrates a Bluetooth 5 radio with an ARM® Cortex® M0 processor, RF Energy Harvester, and state-of-the-art energy management to enable “forever battery” and battery free operation in low-power devices.

With its ability to harvest energy from multiple sources and manage energy storage, the ATM3 is a flexible SoC solution for wide range of products across consumer, commercial, and industrial Internet of Things (IoT) markets.

The ATM3 series is available in a 40 pin QFN package (ATM3201) or 64 pin DR-QFN package (ATM3221) supporting additional I/O pins.

Applications

Industrial and Enterprise

- Beacons
- Remote Sensors
- Environmental Monitors

Healthcare

- Asset Trackers
- Locationing
- Wearables

Home

- Home Automation
- Remote Control
- Human Interface Devices (HID)
- Entertainment

Smart Cities

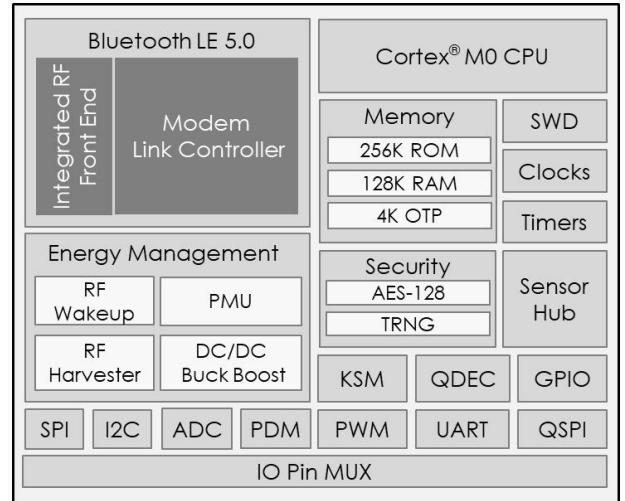
- Asset Trackers
- Beacons

Personal

- Gaming
- Wearables

Auto

- Key fobs and Accessories
- Infotainment



Features

- On-chip **RF Energy Harvesting** with dedicated antenna input
- Supports **Photovoltaic, Thermal, Motion** and other energy harvesting technologies
- Bluetooth LE 5.0 compliant
- Fully integrated RF front-end
- 16 MHz ARM® Cortex® M0 CPU
- 256 KB ROM, 128 KB RAM, 4 KB OTP
- SWD for interactive debugging
- External Harvesting/Storage Interface
- Integrated Power Management Unit (PMU)
- DC/DC Buck-Boost Converter
- RF Wakeup Receiver
- I2C, SPI, UART, PWM Peripherals
- Configurable GPIOs
- Quad SPI with Execute in Place (XIP)
- Application ADC (10-bit)
- Digital microphone input (PDM)
- Keyboard matrix controller (KSM)
- Quadrature decoder for mouse input (QDEC)
- 16 MHz / 32.768 kHz Crystal Oscillator
- AES 128 hardware
- True random number generator (TRNG)
- Sensor Hub

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The ATM3 product family has on-chip **RF Energy Harvester** with a dedicated antenna port as well as a separate input for energy from photovoltaic, mechanical and thermal harvesting devices.

The **Power Management Unit** controls the harvesting and energy storage elements to optimize the sourcing of core and I/O power. Constant monitoring regulates chip operation based on harvested and stored energy.

An integrated **Sensor Hub** is a configurable hardware element that can read data from external sensors and write to an external flash device on the quad SPI interface while all other power domains are powered down. The sensor hub can also trigger a wakeup of the CPU if the data read falls outside programmed thresholds.

The independent **RF Wakeup Receiver** is designed to look for an incoming paging or wakeup signal while the rest of the SoC remains in a very low power state. The receiver is designed for short range reception of a configurable signal from a Bluetooth device, mobile phone, or dedicated transmitter.

The extensive set of **Peripherals** on the ATM3 includes multiple UART cores, two I2C masters, two general purpose SPI masters, and a separate Quad SPI capable of supporting an external flash mapped directly to the CPU. Dedicated hardware supports a Pulse Density Modulated (PDM) digital microphone, multiple Pulse Width Modulation (PWM) outputs, Quadrature decoder (QDEC) for mouse inputs, Keyboard Matrix Controller (KSM), Analog Comparator, and Application ADC. Flexible pin muxing allows the needed signals to be routed to the I/O pins based on the application and product requirements.

A complete **Software Development Environment** allows developers to customize the existing ROM-based application or to develop a custom application that runs from external memory.

Available directly from Atmosic, an **Evaluation Kit** for both package variants supports performance evaluation, software customization, and complete product development.

Specifications

Bluetooth Version	Bluetooth LE 5.0
Data Rates Supported	2 Mb/s, 1 Mb/s, 500 kb/s, 125 kb/s
Output Power	-20 dBm to +4 dBm
Receive Sensitivity	-95 dBm @ 1 Mb/s
Input Voltage	1.1 V to 3.3 V
Power Consumption@ 3 V	1.0 mA RX @-95 dBm 2.5 mA TX @0 dBm
CPU	16 MHz ARM® Cortex® M0 processor
On-Chip Memory	256 KB ROM, 128 KB RAM, 4 KB OTP
RAM Retention	16 KB to 128 KB in 16 KB steps
RF Energy Harvester	-7.5 dBm to 7.0 dBm input 900 MHz, 2.4 GHz RF Bands
Security Hardware	AES-128, True Random Number Generator (TRNG)
GPIO	30 available on DR-QFN 16 available on QFN
Timers	4 General Purpose with separate dedicated Wakeup Timer.
Peripherals	I2C, SPI, QSPI, UART, PDM, PWM, QDEC, KSM, ADC
Operating Temperature Range	-40° C to +85° C
Package Options	ATM3201: 5x5 mm 40-pin QFN ATM3221: 6x6 mm 64-pin DR-QFN

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